AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A method for persistently tracking volatile memory faults, the method comprising:
detecting a memory error relating to at least one dynamic random access memory (DRAM) unit on a particular memory module; and
writing an entry pertaining to the memory error in non-volatile memory of [[an]] a fault storage unit on [[that]] the particular memory module,
wherein the entry comprises a DRAM unit identifier, a start bit of the memory error, an end bit of the memory error, and tag bits indicating time of last failure and number of occurrences of failure.

2. (original) The method of claim 1, wherein the particular memory module comprises a particular dual in-line memory module (DIMM) of a plurality of DIMMs in a memory system.

3. (original) The method of claim 1, further comprising:
determining a scope of the detected memory error.

4. (currently amended) The method of claim 3, wherein the scope of the memory error is determined by [[a logical analysis of]] using a history of faults associated with the particular memory module.

5. (canceled)

6. (original) The method of claim 1, further comprising:

reading the entry from the non-volatile memory of the fault storage unit; and

removing memory bits associated with the memory error from a set of usable memory.

7. (original) The method of claim 1, further comprising:

removing memory bits associated with the memory error from a set of usable memory while the particular memory module remains online.

8. (currently amended) A memory module that persistently tracks volatile memory faults, the memory module comprising:

a plurality of dynamic random access memories (DRAMs); and

a fault storage unit including non-volatile memory configured to store entries pertaining to faults in the plurality of DRAMs on that memory module,

wherein each said entry comprises a DRAM unit identifier, a start bit of a memory error, an end bit of the memory error, and tag bits indicating time of last failure and number of occurrences of failure.

9. (original) The memory module of claim 8, further comprising:

interface circuitry configured to provide read and write access by a memory error interface unit on a circuit board to the non-volatile memory of the fault storage unit.

10. (original) The memory module of claim 8, wherein an entry stored in the non-volatile memory of the fault storage unit includes a DRAM identifier and a range of bits.

11. (original) The memory module of claim 8, wherein the memory module comprises a dual in-line memory module (DIMM).

12. (currently amended) A circuit board of a system, the circuit board comprising:

a plurality of connectors, each connector ~~configured to connect to~~ connects to a memory module which includes multiple volatile memory units and a non-volatile fault storage unit;

a memory controller configured to read and write data into the volatile memory units of memory modules; [[and]]

a memory error interface configured to provide read and write access to the non-volatile fault storage units of the memory modules; and

error handling code including instructions to write entries relating to detected memory errors into the non-volatile fault storage unit and to read said entries from the non-volatile fault storage unit,

wherein each said entry comprises a memory unit identifier, a start bit of a memory error, an end bit of the memory error, and tag bits indicating time of last failure and number of occurrences of failure.

13. (original) The circuit board of claim 12, further comprising:

a processor dependent hardware (PDH) interface communicatively coupled between a central processing unit and the memory error interface.

14. (currently amended) The circuit board of claim 13, further comprising:

a processor dependent code (PDC) unit accessible via the PDH interface, wherein the PDC unit includes boot code and said error handling code.

15. (original) The circuit board of claim 14, wherein the boot code includes instructions to read the entries from the non-volatile fault storage unit and to remove memory bits associated with the entries from a set of usable memory.

16. (canceled)

17. (original) The circuit board of claim 12, wherein the volatile memory units comprise dynamic random access memory, and wherein the plurality of memory modules comprise dual in-line memory modules (DIMMs).

18. (currently amended) A memory system comprising:
means for reading data from and writing data to volatile memory units on a plurality of memory modules; and
means for reading error entries from and writing error entries to a non-volatile fault storage unit on each memory module,
wherein an error entry comprises a DRAM unit identifier, a start bit of a memory error, an end bit of the memory error, and tag bits indicating time of last failure and number of occurrences of failure.